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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,408	11/13/2001	Michael Purtell	ADTST.037AUS	2970

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EXAMINER

KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

24

Office Action Summary

Application No.

10/008,408

Applicant(s)

PURTELL ET AL.

Examiner

James C Kerveros

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 May 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☒ Claim(s) 2, 4 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 2, 4 and 6 are objected to because of the following informalities:

Claims 2, 4 and 6 require indentation. Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(m).

Claim 6, line 5, the term "overall" should be deleted because it renders the claim indefinite for failing to properly define the limitation of the "illustration of the test pattern".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Huston et al. (US 6079038), issued: June 20, 2000.

Regarding Claim 1, Huston discloses a semiconductor test system (40, FIG. 5) for producing a Shmoo plot contour graph displaying operating parameters and test results for an integrated circuit device under test (DUT) 42, comprising:

Means (tester, 44) for generating a test pattern and applying the test pattern to a semiconductor device under test DUT (42).

Means (tester 44), for evaluating a response output of the semiconductor DUT, collecting test result data, and transmits pass/fail data back to host computer 46 via bus 47 indicating whether DUT 42 passed or failed the test, FIG. 5.

Host computer (46) for controlling the overall operation of the test system, by instructing the tester 44 to repeatedly perform the same test on DUT 42 using different combinations of values, and for generating a Shmoo plot on display monitor 48 or paper printer by a printer 45.

Wherein the host computer displays a device characterization map "Shmoo plot", as illustrated, FIG. 1, graphically distinguishing the combinations of operating parameter values, for which the DUT 42 operates correctly or fails to operate correctly, such as (PASS/ FAIL), where the Shmoo plot has a multi-dimensional, horizontal X, Y axis corresponding to the operating parameters.

Regarding Claim 5, Huston discloses a characterization map, which includes:

A margin map plot (FIG. 6), which shows pass/fail points for individual pins for a DUT corresponding to parameters values within an area of interest bounded by minimum and maximum values of X and Y, (XMIN, YMIN, and XMAX, YMAX).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huston et al. (US 6079038) in view of Ullmann (US 5731984).

Regarding Claims 2, 3, 4 and 6, Huston discloses a characterization map, which includes:

A checkerboard map (Shmoo plot, FIG. 1), having horizontal and vertical (X, Y) axis representing test operating parameters, such as pins for the horizontal (X) axis corresponding to voltage and time for the vertical (Y) axis corresponding to clock frequency for DUT (42, FIG. 5).

A shmoo plot FIG. 2, which shows pass symbol 18 if the DUT fails the test /fail symbol 20 if the DUT fails the test at the appropriate plot coordinates (X and Y) for a single device under test, DUT.

A composite map (shmoo plot FIG. 1) representing the horizontal and vertical (X, Y) test data for one DUT under test, which is identical to plurality of devices under test, DUTs.

A margin map plot (FIG. 6), which shows pass/fail points for individual pins for a DUT corresponding to parameters values within an area of interest bounded by minimum and maximum values of X and Y, (XMIN, YMIN, and XMAX, YMAX).

Regarding Claims 2 and 6, Huston does not explicitly disclose a waveform display, which shows a test pattern to be applied to the device under test based on the event data from the event memory.

Ullmann (US 5731984), in an analogous art, discloses a waveform image on display 18, FIG. 1, corresponding to test vector pattern repetitively applied to the device under test (DUT 20). FIG. 14 shows an example of the acquisition of waveform data corresponding to vectors 26-37, representing the waveform 1410 appearing on net 28 of the DUT. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply a waveform image, as taught by Ullmann, on Huston's display monitor (48, FIG. 5), which corresponds to a test vector pattern for a DUT, for the purpose of enhancing the graphical presentation, since Huston already employs an existing display monitor with associated video driver software, which is compatible with existing software executed by the host computer (46, FIG. 5) for waveform display.

Regarding Claims 3 and 4, Huston does not explicitly disclose expanding the time scale of the checkerboard map. However, in an analogous art, in conventional waveform acquisition, Ullmann (US 5731984) displays an oscilloscope-like image 32 in a window of terminal display 18 showing the acquired waveform in time domain (amplitude or logic level vs. time), beginning at a time following the trigger. The display is equipped with time delay, which is capable of enlarging the time scale by zooming the image, like in a typical oscilloscope, FIGS. 15-18. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the time

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delay feature, as taught by Ullmann , with Huston's display monitor (48, FIG. 5), for the purpose of enhancing the graphical presentation, since Huston already employs an existing display monitor with associated video driver software, which is compatible with existing software executed by the host computer (46, FIG. 5) for waveform display.

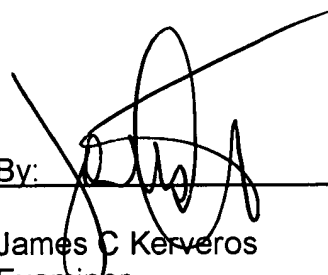
Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 2 April 2004
Office Action: Non-Final Rejection

By: 
James C Kerveros
Examiner
Art Unit 2133


for

Albert DeCady
Primary Examiner